

# MEASUREMENT AND ANALYSIS OF A FERROELECTRIC FIELD-EFFECT TRANSISTOR NAND GATE

THOMAS A. PHILLIPS<sup>a</sup>, TODD C. MACLEOD<sup>a</sup>, RANA SAYYAH<sup>b</sup>, and FAT DUEN HO<sup>b</sup>

*<sup>a</sup>National Aeronautics and Space Administration, Marshall Space Flight Center,  
Huntsville, Alabama, 35812, U.S.A.*

*<sup>b</sup>The University of Alabama in Huntsville, Department of Electrical and Computer Engineering,  
Huntsville, Alabama 35899, U.S.A.*

## ABSTRACT

Previous research investigated expanding the use of Ferroelectric Field-Effect Transistors (FFET) to other electronic devices beyond memory circuits. Ferroelectric based transistors possess unique characteristics that give them interesting and useful properties in digital logic circuits. The NAND gate was chosen for investigation as it is one of the fundamental building blocks of digital electronic circuits. In this paper, NAND gate circuits were constructed utilizing individual FFETs. N-channel FFETs with positive polarization were used for the standard CMOS NAND gate n-channel transistors and n-channel FFETs with negative polarization were used for the standard CMOS NAND gate p-channel transistors. The voltage transfer curves were obtained for the NAND gate. Comparisons were made between the actual device data and the previous modeled data. These results are compared to standard MOS logic circuits. The circuits analyzed are not intended to be fully operational circuits that would interface with existing logic circuits, but as a research tool to look into the possibility of using ferroelectric transistors in future logic circuits. Possible applications for these devices are presented, and their potential benefits and drawbacks are discussed.

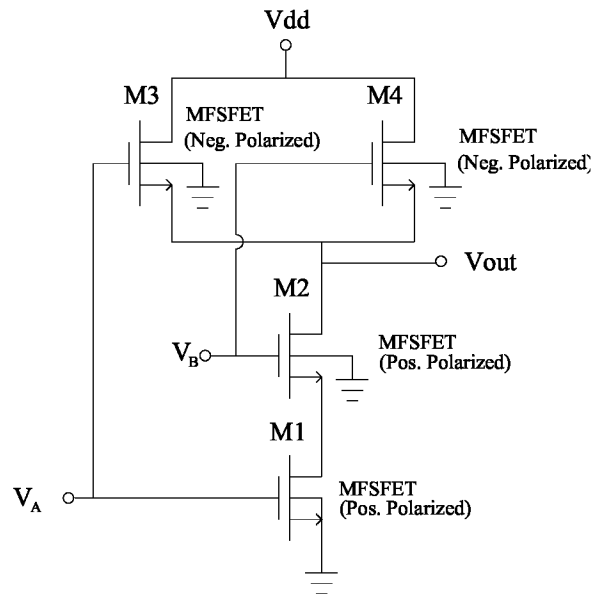


Figure 1: 2-Input MFSFET NAND Gate

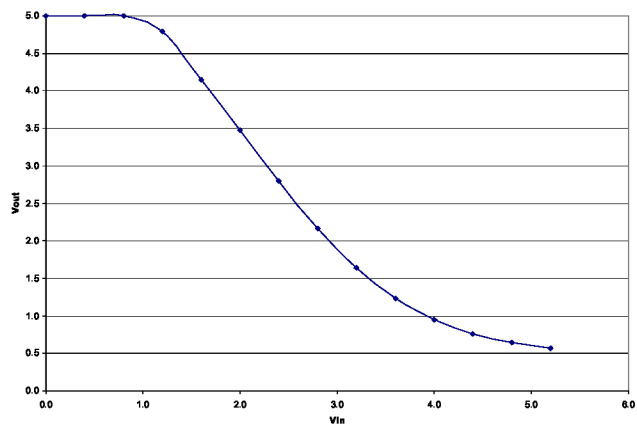


Figure 2: Voltage Transfer Curve for MFSFET Inverter

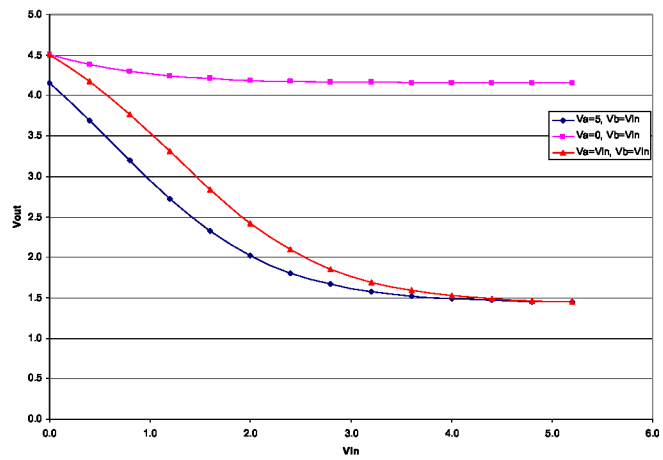


Figure 3: Voltage Transfer Curve for 2-Input MFSFET NAND Gate